AMENDMENT TO THE CLAIMS

1. to 14. (Cancelled)

15. (New) An image processing apparatus comprising:

first and second coding units each capable of at least encoding image data; and

first and second buses connected respectively to said first and second coding units and to a switching control unit which is connected by a third bus to an image memory unit adapted to store image data,

wherein said switching control unit is adapted to control access from said first and second coding units to said image memory unit by providing a first data transfer channel between said first bus and said third bus and a second data transfer channel between said second bus and said third bus simultaneously so that image data coding by said first coding unit and image data coding by said second coding unit can be executed in parallel.

16. (New) An apparatus according to claim 15, wherein at least one of said first coding unit and said second coding unit are also capable of decoding image data.

17. (New) An apparatus according to claim 15, wherein said switching control unit further comprises:

a memory control unit, connected to said third bus, adapted to control said image memory unit; and

a bus control unit connected to said first and second buses and further connected to said memory control unit through a fourth bus.

18. (New) An apparatus according to claim 17, further comprising:

an image interface unit adapted to connect the image processing apparatus to an image input apparatus or an image output apparatus and transmit the image data to said image output apparatus or receive the image data from said image input apparatus; and

a transfer control unit adapted to control the image data transfer between said image memory unit and said apparatus connected to said image interface unit through said switching control unit.

19. (New) An apparatus according to claim 18, wherein said switching control unit further has a cache memory.

20. (New) An apparatus according to claim 18, wherein said transfer control unit is adapted to discriminate the amount of image data stored in said image memory unit so that in a case where said image data amount reaches an amount by which a connected image output apparatus can output an image at a predetermined speed irrespective of the difference of processing speeds between said image input apparatus and said image output apparatus, and said image processing apparatus transfers image data from said image memory unit to said connected image output apparatus through said switching control unit.

21. (New) An apparatus according to claims 15, wherein said switching control unit comprises a crossbar switch.

22. (New) A method of executing image processing on a image processing apparatus having first and second coding units each capable of encoding image data connected to first and second buses connected to a switching control unit connected by a third bus to an image memory unit, said method comprising:

an access control step of controlling access from said first and second coding units to said image memory unit by providing a first data transfer channel between said first bus and said third bus and a second data transfer channel between said second bus and said third bus simultaneously; and

an executing step of executing image data coding by said first coding unit and image data coding by said second coding unit in parallel.

23. (New) A method according to claim 22, wherein at least one of said first coding unit and said second coding unit are also capable of decoding image data.

24. (New) A method according to claim 23, further comprising:

a connecting step of connecting the image processing apparatus to an image input apparatus;

a receiving step of receiving the image data from said image input apparatus; and

a transfer control step of controlling the image data transfer between said image memory unit and said image input apparatus connected to the image processing apparatus in said connecting step.

25. (New) A method according to claim 23, further comprising:

a connecting step of connecting the image processing apparatus to an image output apparatus;

a transmitting step of transmitting the image data to said image output apparatus; and

a transfer control step of controlling the image data transfer between said image memory unit and said image output apparatus connected to the image processing apparatus in said connecting step.

26. (New) A method according to claim 24, further comprising the step of:

a discriminating step of discriminating the amount of image data stored in said image memory unit so that in a case where said image data amount reaches an amount by which a connected image output apparatus can output an image at a predetermined speed irrespective of the difference of processing speeds between said image input apparatus and said image output apparatus, the image data being transferred from said image memory unit to said connected image output apparatus through said switching control unit.

27. (New) An image processing apparatus comprising:

a first coding unit adapted to encode image data;

a second coding unit adapted to encode image data;

an image memory unit adapted to store image data;

a switching unit adapted to switch connection from said image memory unit to said first coding unit or said second coding unit;

a first bus adapted to connect said first coding unit to said switching unit;

a second bus adapted to connect said second coding unit to said switching unit; and

a third bus adapted to connect said image memory unit to said switching unit,

wherein said switching unit switches connection from said image memory unit to said first coding unit or said second coding unit so that encoding by said first coding unit and encoding by said second coding unit are executed in parallel.

28. (New) An apparatus according to claim 27, wherein at least one of said first coding unit and said second coding unit is also adapted to decode image data.